ELECTRONIC INFORMATION DISCLOSURE STATEMENT

Electronic Version v18

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Title of Invention	COMPLIANT PASSIVATED EDGE SEAL FOR LOW-K INTERCONNECT STRUCTURES

Application Number :

Confirmation Number:

First Named Applicant: Daniel Edelstein

Attorney Docket Number: FIS920030255US1

Art Unit:

Examiner:

Search string: (5742094 or 6538214 or 6372527 or 5679977 or 6271578 or 5665655 or 6383893 or 20020117759).pn

US Patent Documents

Note: Applicant is not required to submit a paper copy of cited US Patent Documents

init	Cite.No.	Patent No.	Date	Patentee	Kind	Class	Subclass
	1	5742094	1998-04-21	Ting			
	2	6538214	2003-03-25	Khandros			
	3	6372527	2002-04-16	Khandros, et al.			
	4	5679977	1997-10-21	Khandros, et al.			
	5	6271578	2001-08-07	Mitwalsky, et al.			
	6	5665655	1997-09-09	White			
	7	6383893	2002-05-07	Begle, et al.			

US Published Applications

Note: Applicant is not required to submit a paper copy of cited US Published Applications

init	Cite.No.	Pub. No.	Date	Applicant	Kind	Class	Subclass
	1	20020117759	2002-08-29	Bauch, et al.			

Signature

Examiner Name	Date
	11/1/04

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PATENT & TRADEMARK OFFICE

INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

Docket Number (Optional)	Application Number
FIS920030255US1	10/707,713
Applicant(s)	
Daniel C. Edelstein, et al.	
Filing Date	**Group Art Unit**
1/6/04	Not Yet Assigned

EXAMINER INITIAL		OTHER DOCUMENTS *(Including Author, Title, Date, Pertinent Pages, Etc.)*
DW		H. A. Reed et al., "Compliant Wafer Level Package (CWLP) With Embedded Air-Gaps For Sea of Leads (SoL) Interconnections," Proc. of IEEE 2001 International Interconnect Technology Conference, pp. 151-153.
		M.S. Bakir et al., "Sea of Leads Microwave Characterization and Process Integration with FEOL and BEOL," Proc. of IEEE 2002 International Interconnect Technology Conference, pp. 116-118.
		A. Mule et al., "Optical Waveguides With Embedded Air-Gap Cladding Integrated Within a Sea-of-Leads (SoL) Wafer-Level Package," Proc. of IEEE 2002 International Interconnect Technology Conference, pp. 122-124.
		"Chip Pad Process" IBM Technical Disclosure bulletin, Oct. 1991.
		"Via Reliability Problem Eliminated by an Offset Elliptical Via," IBM Technical Disclosure Bulletin, Jan. 1998, pp. 310-311
DW		"Structure for the Passivation of Semiconductor Chips," IBM Technical Disclosure Bulletin, Aug. 1973, p. 728

EXAMINER	DATE CONSIDERED
	11/1/04

*EXAMINER: Initial if citation considered, whether or not citation is in conformance with MPEP Section 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.